



100Gb/s CFP2 Optical Transceiver

RTXM290-608

Features

- Direct LC receptacle optical interface
- Single +3.3V power supply
- Hot-pluggable
- Operating optical data rate up to 112Gbps
- Transmission distance up to 40km
- AC coupling of CML signals
- 1310 nm window cooled EA-DFB LD
- Integrated SOA, PIN ROSA and TOSA
- Low power dissipation(Max:9W)
- Built in digital diagnostic function
- Operating case temperature range:0 ℃ to 70 ℃
- Compliant with RoHS
- MDIO Communication Interface

Application

- Local and wide area network (LAN and WAN)
- Ethernet switches and router applications
- ITU-T OTU4 OTL4.4 applications

Standards

Output Low Voltage ($I_{OL}=100\mu A$)	3.3VOL	V		0.2
Minimum Pulse Width of Control Pin Signal	t_{CNTL}	us	100	
1.2V LVCMOS Electrical Characteristics				
Input High Voltage	1.2VIH	V	0.84	1.5
Input Low Voltage	1.2VIL	V	-0.3	0.36
Input Leakage Current	1.2IIN	μA	-100	+100
Output High Voltage	1.2VOH	V	1.0	1.5
Output Low Voltage	1.2VOL	V	-0.3	0.2
Output High Current	1.2IOH	mA		-4
Output Low Current	1.2IOL	mA	+4	
Input Capacitance	Ci	pF		10
Optical transmitter Characteristics				
Signaling Rate for Each Lane (100GbE)			-	25.78125
Signaling Rate for Each Lane (OTU4)		Gbps		27.95249
Four Lane Wavelength Range	λ_1	nm	1294.53	1295.56 1296.59
	λ_2		1299.02	1300.05 1301.09
	λ_3		1303.54	1304.58 1305.63
	λ_4		1308.09	1309.14 1310.19
Side Mode Suppression Ratio	SMSR	dB	30	-

Time					“OR” of Associated MDIO alarm& status registers.Please see MDIO document for further details
Global Alarm De-assert Delay Time	De-assert	GLB_ALRMn_deassert		150 ms	

Differential Voltage						Differential
RMS jitter ^{1,2}	σ			10	ps	Random Jitter Over frequency band of 10KHz<f<10MHz
Clock Duty Cycle		40		60	%	
Clock Rise/Fall Time 10%/90%	$t_{r/f}$	200		1250	ps	1/64 of electrical lane rate
		50		315		1/16 of electrical lane rate

Optional Transmitter and Receiver Monitor Clock Characteristics

		Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency					MHz	1/8 of Network lane rate
Output Differential Voltage	V _{DIFF}	400		1200	mV	Peak to Peak Differential
Clock Duty Cycle		40		60	%	

CFP Register Allocation

CFP Register Allocation					
Starting Address in Hex	Ending Address in Hex	Access Type	Allocated Size	Data Bit Width	Table Name and Description
0000 8000	7FFF 807F	N/A RO	32768	N/A	Reserved for IEEE 802.3 use

B000	FFFF	RO	5x4096	N/A	Reserved by CFP MSA
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CFP NVR1

CFP NVR1						
Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
8000	1	RO	7~0	Base ID Information Module Identifier	11	N/A

806E	1	RO	7~0	Digital Diagnostic Monitoring Type	C	N/A
806F	1	RO	7~0	Digital Diagnostic Monitoring Capability 1	3	N/A
8070	1	RO	7~0	Digital Diagnostic Monitoring Capability 2	F	

80BA	2	RO	7~0	Laser Temperature High Warning Threshold	3C	SeeA2C0h
80BC	2	RO	7~0	Laser Temperature Low Warning Threshold	28	SeeA2C0h
80BE	2	RO	7~0	Laser Temperature Low Alarm Threshold	23	SeeA2C0h

		RW	7~0	Alarm Source Code		
A009	1	RO		PRG_ALARM2 Source Select	0002h	
			15~8	Reserved		
		RW	7~0	Alarm Source Code		
A00A	1	RO		PRG_ALARM1 Source Select	0001h	
			15~8	Reserved	00h	
		RW	7~0	Alarm Source Code	00h	
A00B	1	RO		Module Bi-/Uni-Directional Operating Mode Select	0000h	
			15~3	Reserved	0	
		RW	2~0	Module Bi/uni-Directi	9.767.52 0.4799	

A013	1	RW		Individual Network Lane TX_DIS Control	0000h	
			15	Lane 15 Disable	0	
			14	Lane 14 Disable	0	
			13	Lane 13 Disable	0	
			12	Lane 12 Disable	0	
			11	Lane 11 Disable	0	
			10	Lane 10 Disable	0	
			9	Lane 9 Disable	0	
			8	Lane 8 Disable	0	
			7	Lane 7 Disable	0	
			6	Lane 6 Disable	0	
			5	Lane 5 Disable	0	
			4	Lane 4 Disable	0	
			3	Lane 3 Disable	0	
			2	Lane 2 Disable	0	
			1	Lane 1 Disable	0	
			0	Lane 0 Disable	0	
A014						

[illegible]

			8	Lane 8 Fault and Status Summary	0	
			7	Lane 7 Fault and Status Summary	0	
			6	Lane 6 Fault and Status Summary	0	

			2	Mod Aux 2 High Warning	0	
			1	Mod Aux 2 Low Warning	0	
			0	Mod Aux 2 Low Alarm	0	
A021	1	RO		Reserved	0000h	
A022	1			Module State Latch	0000h	
		RO	15~9	Reserved	0	
		RO/LH/COR	8	High-Power-down State Latch	0	
		RO/LH/COR	7	TX-Turn-off State Latch	0	
		RO/LH/COR	6	Fault State Latch	0	
		RO/LH/COR	5	Ready State Latch	0	
		RO/LH/COR	4	TX-Turn-on State Latch	0	

		RO/LH/COR	5	Mod Aux 1 Low Warning Latch	0	
		RO/LH/COR	4	Mod Aux 1 Low Alarm Latch	0	
		RO/LH/COR	3	Mod Aux 2 High Alarm Latch	0	
		RO/LH/COR	2	Mod Aux 2 High Warning Latch	0	
		RO/LH/COR	1	Mod Aux 2 Low Warning Latch	0	
		RO/LH/COR	0	Mod Aux 2 Low Alarm Latch	0	
A027	1	RO		Reserved	0000h	
A028	1			Module Stable Enable	006Ah	
		RO	15~9	Reserved	0	
		RW	8	High-Power-down State Enable	0	
		RW	7	TX-Turn-off State Enable	0	

A02C	1			Module Alarms and Warnings Enable	00FFh	
		RO	15~8	Reserved	00h	
		RW	7	Mod Aux 1 High Alarm Enable	1	
			6	Mod Aux 1 High Warning Enable	1	
			5	Mod Aux 1 Low Warning Enable	1	
			4	Mod Aux 1 Low Alarm Enable	1	
			3	Mod Aux 2 High Alarm Enable	1	
			2	Mod Aux 2 High Warning Enable	1	
			1	Mod Aux 2 Low Warning Enable	1	
			0	Mod Aux 2 Low Alarm Enable	1	
A02D	2	RO		Reserved	0000h	
Module Analog A/D Value Registers						
A02F	1	RO	15~0	Module Temp Monitor A/D Value	0000h	
A030	1	RO	15~0	Module Power supply	0000h	
				3.3 V Monitor A/D Value	0000h	
A031	1	RO	15~0			

A210	16	RO		Network Lane n Fault and Status	0000h	
			15	Lane TEC Fault	0	
			14	Lane Wavelength Unlocked Fault	0	
			13	Lane APD Power Supply Fault	0	
			12~8	Reserved	0	
			7	Lane TX_LOSF	0	
			6	Lane TX_LOL	0	
			5	Reserved	0	
			4	Lane RX_LOS	0	
			3	Lane RX_LOL	0	
			2	Lane RX FIFO error	0	
			1	Reserved	0	
			0	Reserved	0	

CFP Host lane Lane VR1

Host Lane VR1

Host Lane VR1						
Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Host Lane FAWS Status Registers						
A400	16			Host Lane m Fault and Status	0000h	
		RO	15~2	Reserved	0	
		RO	1	Lane TX FIFO Error	0	
		RO	0	TX_HOST_LOL	0	
Host Lane FAWS Latch Registers						
A410	16			Host Lane m Fault and Status Latch	0000h	
		RO	15~2	Reserved	0	
		RO/LH/COR	1	Lane TX FIFO Error Latch	0	
		RO/LH/COR	0	TX_HOST_LOL Latch	0	

Table : CFP2 Pin-Map

1	GND
2	(TX_MCLK _n)
3	(TX_MCLK _p)
4	GND
5	N.C.
6	N.C.
7	3.3V_GND
8	3.3V_GND
9	3.3V
10	3.3V
11	3.3V
12	3.3V
13	3.3V_GND
14	3.3V_GND
15	VND_IO_A
16	VND_IO_B

104	GND
103	N.C.
102	N.C.
101	GND
100	TX3 _n
99	TX3 _p
98	GND
97	TX2 _n
96	TX2 _p
95	GND
94	N.C.
93	N.C.
92	GND
91	N.C.
90	N.C.
89	GND

24	TX_DIS
25	RX_LOS
26	MOD_LOPWR
27	MOD_ABS
28	MOD_RSTn
29	GLB_ALRMn
30	GND
31	MDC
32	MDIO
33	PRTADR0
34	PRTADR1
35	PRTADR2
36	VND_IO_C
37	VND_IO_D
38	VND_IO_E
39	3.3V_GND
40	3.3V_GND
41	3.3V
42	3.3V

81	N.C.
80	GND
79	(REFCLKn)
78	(REFCLKp)
77	GND
76	N.C.
75	N.C.
74	GND
73	RX3n
72	RX3p
71	GND
70	RX2n
69	RX2p
68	GND
67	N.C.
66	N.C.
65	GND
64	N.C.
63	

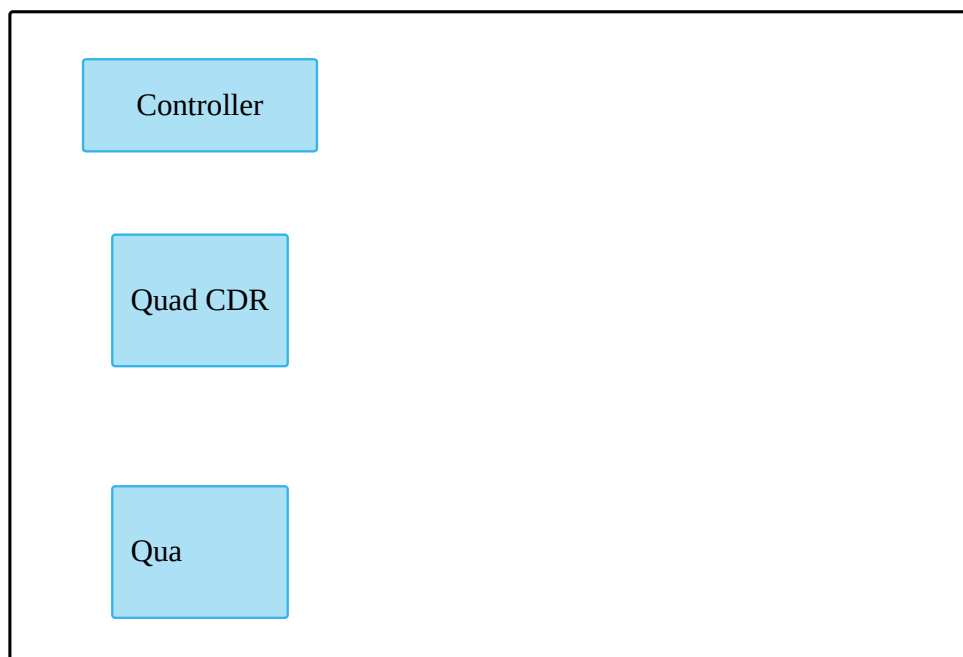
5	N.C.			No Connect
6	N.C.			No Connect
7	3.3V_GND			3.3V Module Supply Voltage Return Ground,can be separate or tied together with Signal
8	3.3V_GND			
9	3.3V			3.3V Module Supply Votage
10	3.3V			

35	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
36	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!

71	GND			
72	RX3p	O	CML	Output Data
73	RX3n	O	CML	Inverted Output Data
74	GND			
75	N.C.			
76	N.C.			
77	GND			
78	(REFCLKp)			
79	(REFCLKn)			



Block diagram





Package outline



Immunity	IEC61000-4-3 Class 2	Compliant with any electro-magnetic regulations
Safety	FDA CDRH 21-CFR 1040 Class 1	
	UL	
	TUV-GS	
	CE	

Ordering Information

Part No	Specifications				Application Code
	Pack	Data rate	Tx	Pout	